

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND1
LAYER 3 : IN1
LAYER 4 : VCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : GND2
LAYER 8 : BOT

BU5D Block Diagram

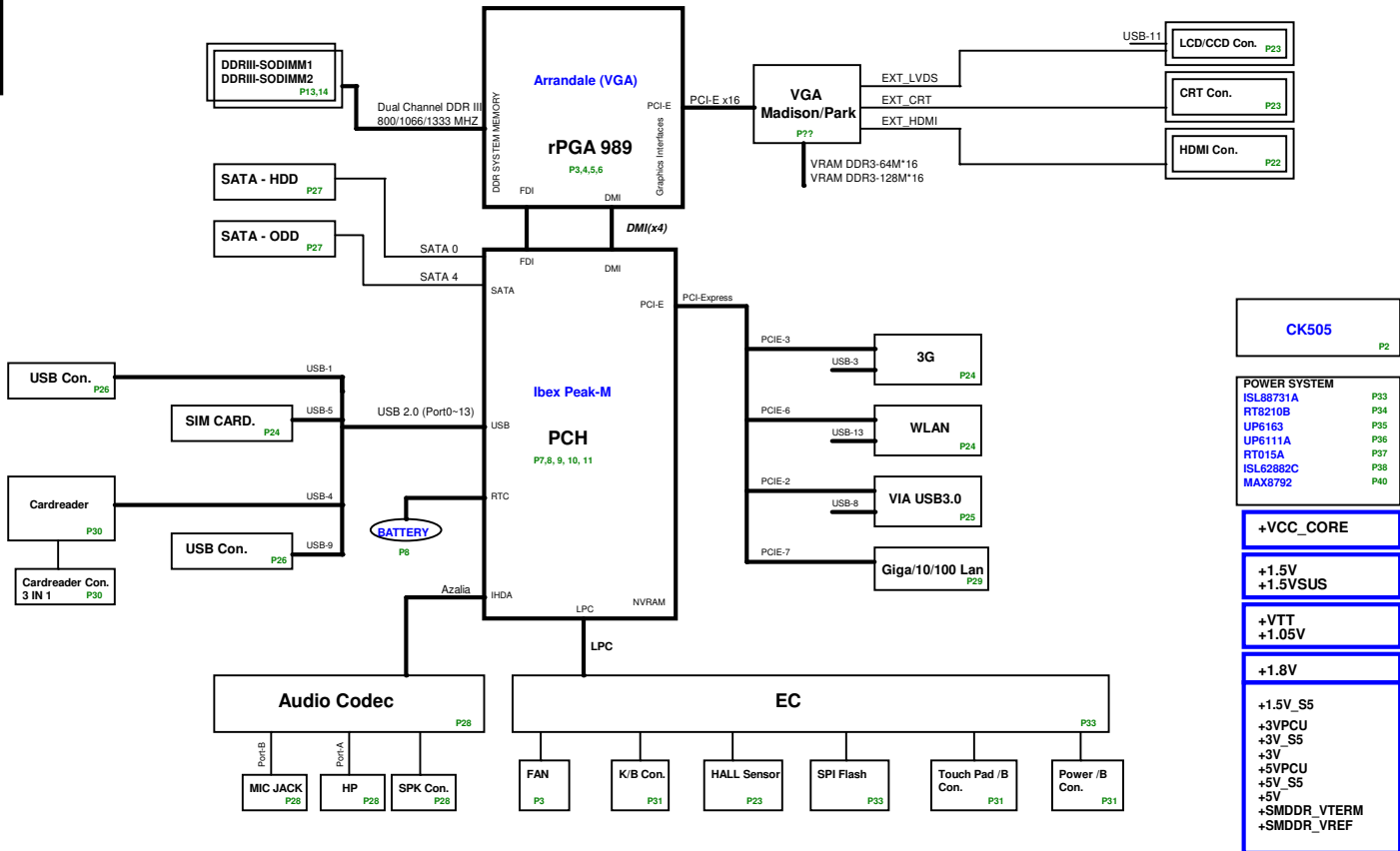







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16	LCD Panel	LDS
	CRT & CRT BUS SWITCH	CRT
	CCD	CCD
	HALL SENSOR&BACK LIGHT SWITCH	HSR
19	Display Port	DPP
20	HDMI comm part	HDM
	HDMI for GM	HMG
21	SATA ODD	ODD
	Main SATA HDD & 2nd SATA HDD	HDD
	G-Sensor	HSD
22	5 IN 1 Card reader	MMC
	IEEE1394	FIW
23	MINI Card (Wi-Fi & WIMAX)	WLN
	MINI Card 2nd	MNC
	MINI Card 3rd	MNC
	TMA Connector	TMA
24	INT KeyBoard & K/B LED Power	KBC
	LED Board	LED
	TP&FP board	TPD,FPD
	Bluetooth Connector	BTM
	Felica Connector	FEC
	MMB Connector	MMB
	Power SW	PSW
	B-CAS Connector	BCS
25	New Card (Express Card)	EXC
	E-SATA comb USB	ESA
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	Light Sensor	LSN
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29	Atheros LAN	LAN
30	NVRAM Connecyoy	NVR
31	Charger (ISL6251A)	PWM
32	System 5V/3V (ISL6237)	PWM
33	CPU CORE (ISL62882)	PWM

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0-S5
+VCCRTC	+3.0V~+3.3V		S0-S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0-S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0-S5
+5VPCU	+5V	AC/DC Insert enable	S0-S5
+5V_TMA	+5V	MAIN_ON	S0
WIMAX_P	+3.3V	WMAX_P for EC	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_S5	+1.5V	S5_ON	S0-S5
+1.5V_SUS	+1.5V	SUSON	S0-S3
+VCC_CORE		VRON	S0
+VTT	+1.05V~+1.1V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		GFXVR_EN	S0

GND PLANE	PAGE
 GND_SIGNAL	32
 CARD_GND	21
 AGND_DC/DC	31
 GND	ALL

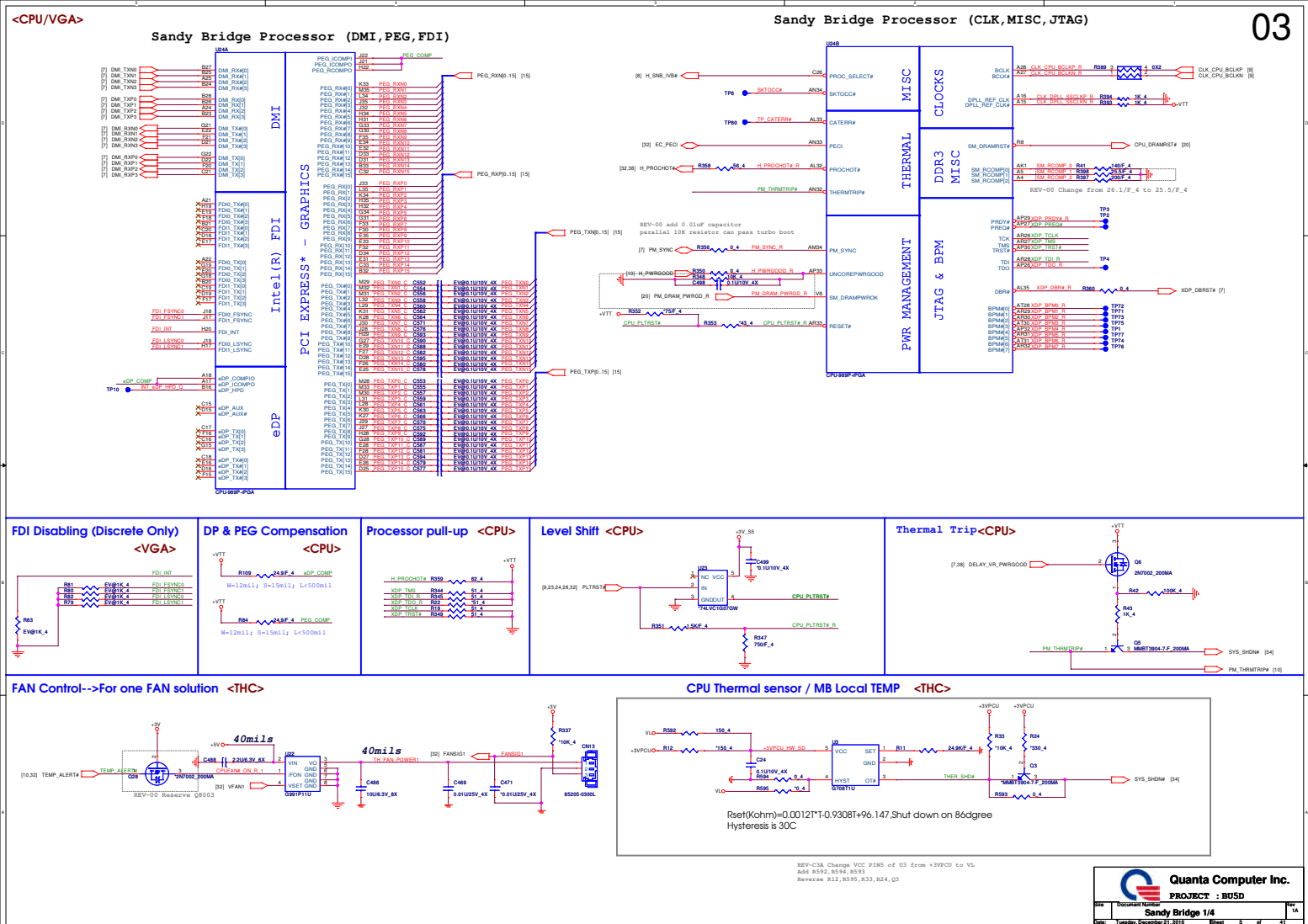
ITEM	Value Code	FUNCTIONS
1	EV@	DISCRETE
2	IV@	UMA
3	U3@	USB 3.0
4	U2@	USB 2.0 (colay W USB 3.0)
5	HM@	HDMI
6	NHM@	No HDMI
7	EHM@	External HDMI
8	3G@	3G
9	C@	Cost issue
10	MDC@	Modem
11	S3@	S3 Power Reduction
12	NS3@	No S3 Power Reduction
13	NGS@	No G-SENSOR
14	51@	1G LAN
15	52@	10/100 LAN
16	GS@	G-SENSOR
17	NMDC@	No Modem

PAGE	DESCRIPTION	BOI-FUNCTIONS
34	VAXG (ISL62881)	PWM
35	+VTT (UP6111A)	PWM
36	+1.05V (UP6111AQDD)	PWM
37	DDR 1.5V (TPS51116)	PWM
38	Discharge (1.5V_S5/1.8V)	PWM
39	Power Tree Table	
40	PCH Power Plane	
41	Power Management	
42	Change List	

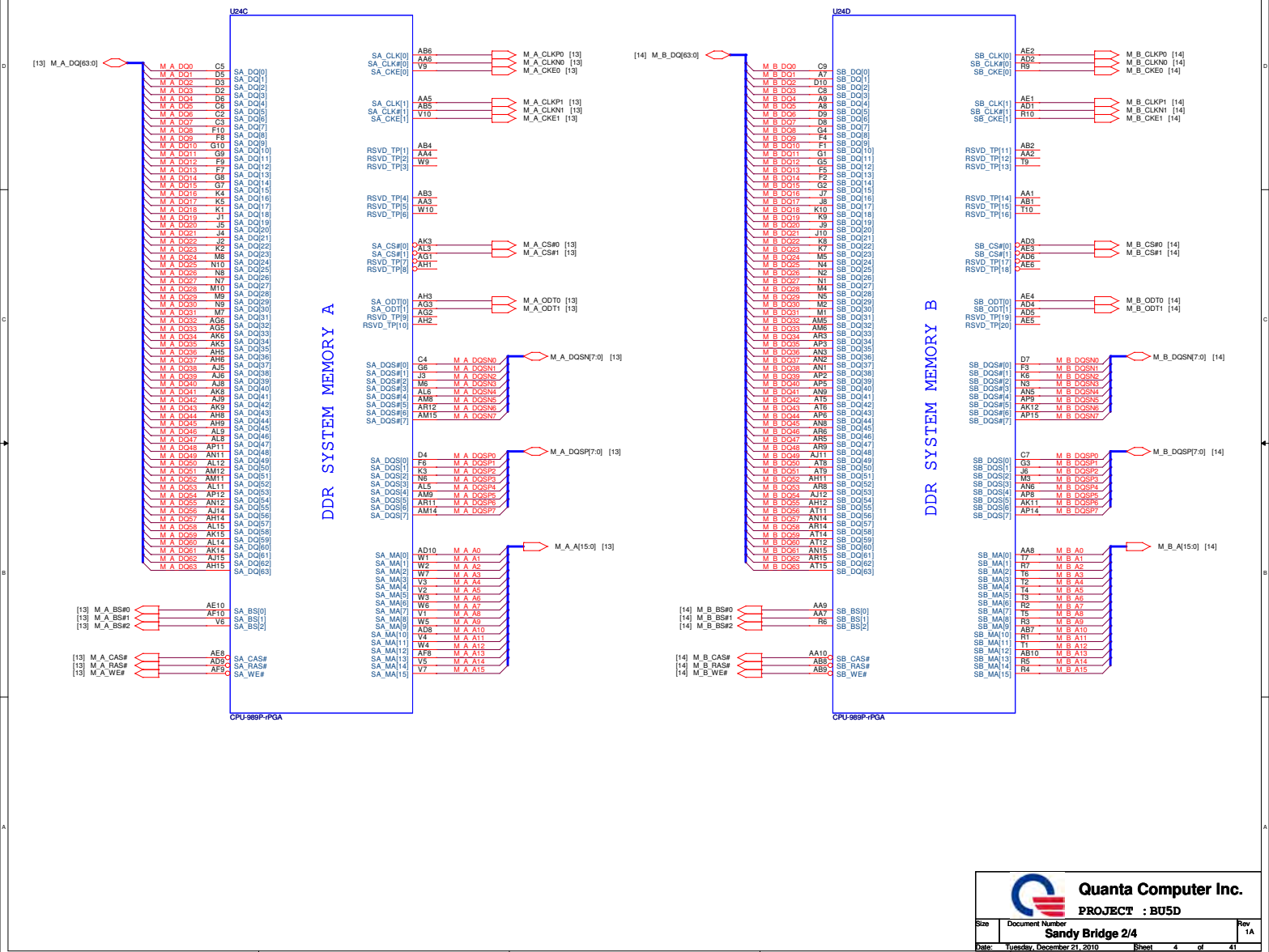



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	POWER STAGE AND BOI-FUNCTION	1A
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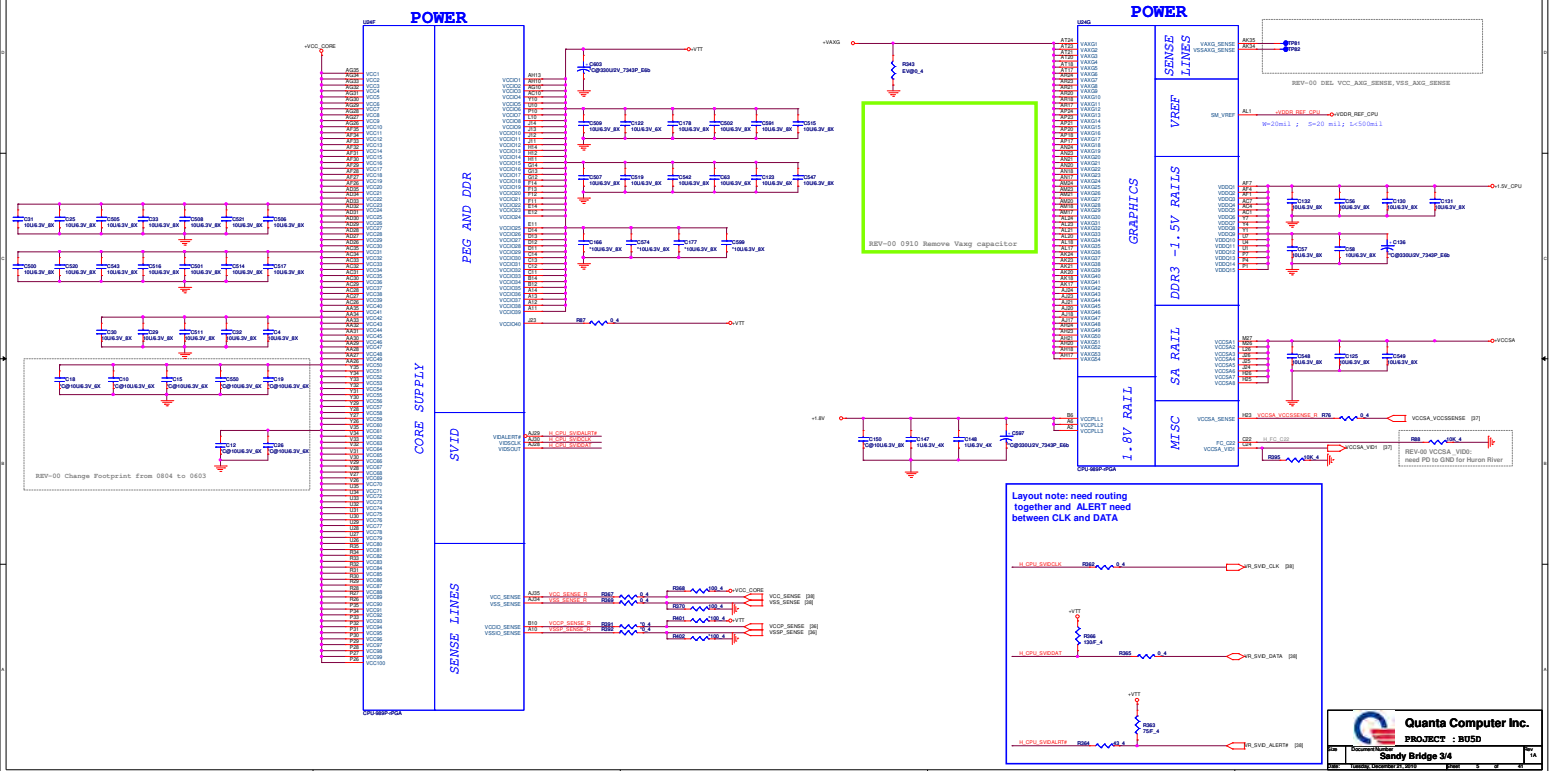
Sandy Bridge Processor (DDR3)





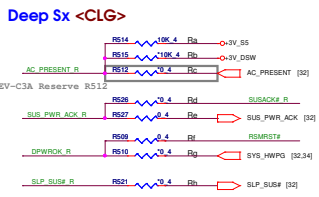
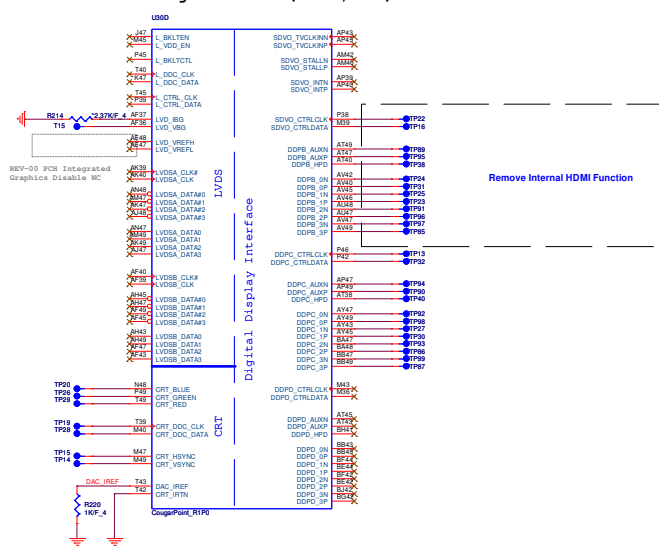
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Size	Document Number	Rev
	Sandy Bridge 2/4	1A
Date:	Tuesday, December 21, 2010	Sheet 4 of 41

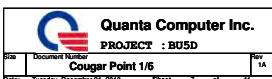


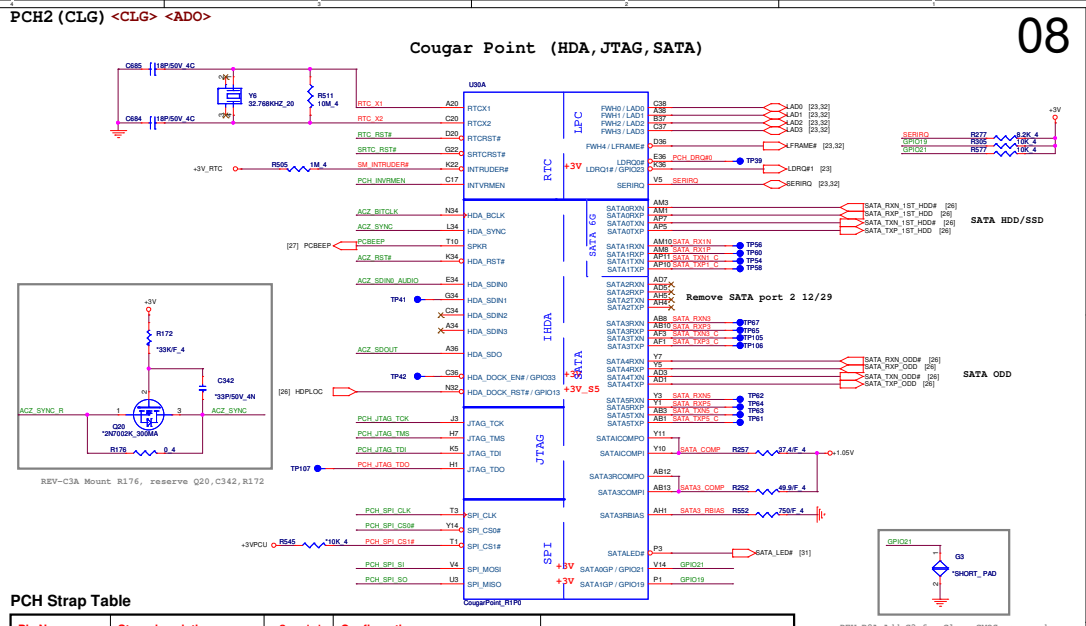
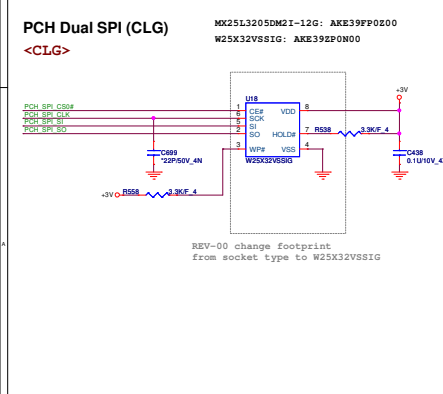
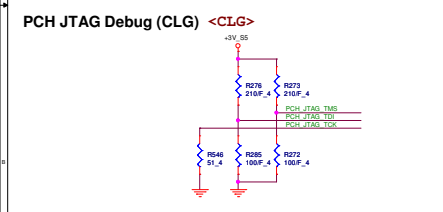
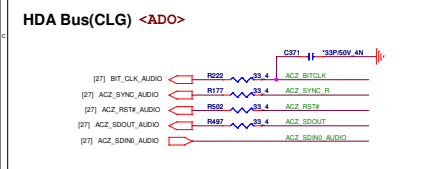
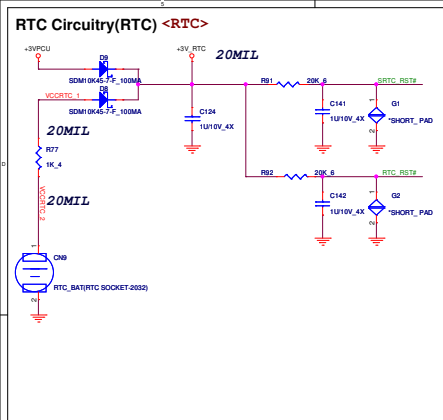
06

Cougar Point (LVDS, DDI)



Net Name	Deep Sx Support	Deep Sx No Support
AC_PRESENT	Rb,Rc stuff	Ra stuff
SUS_PWR_ACK	Rd stuff	Re stuff
DPWROK	Rg stuff	Rf stuff
SLP_SUS	Rh stuff	Rh No stuff

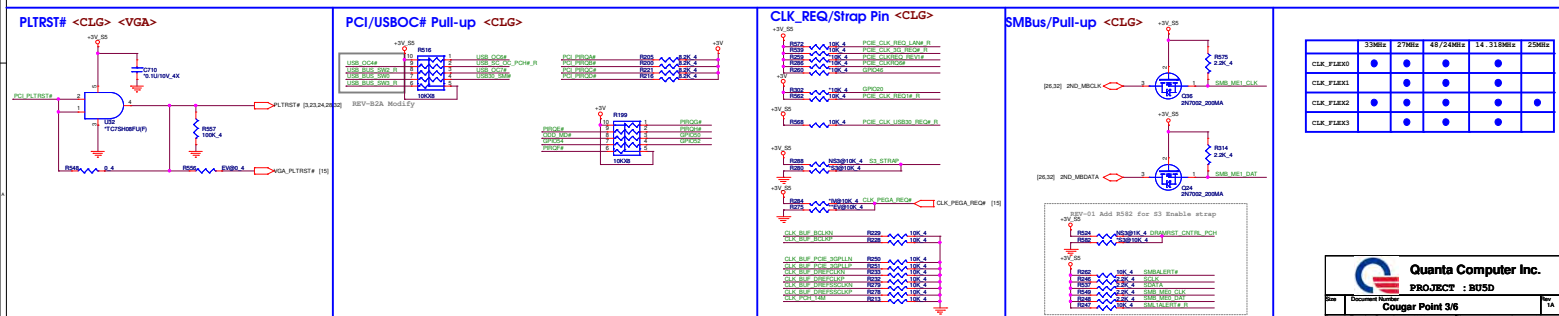




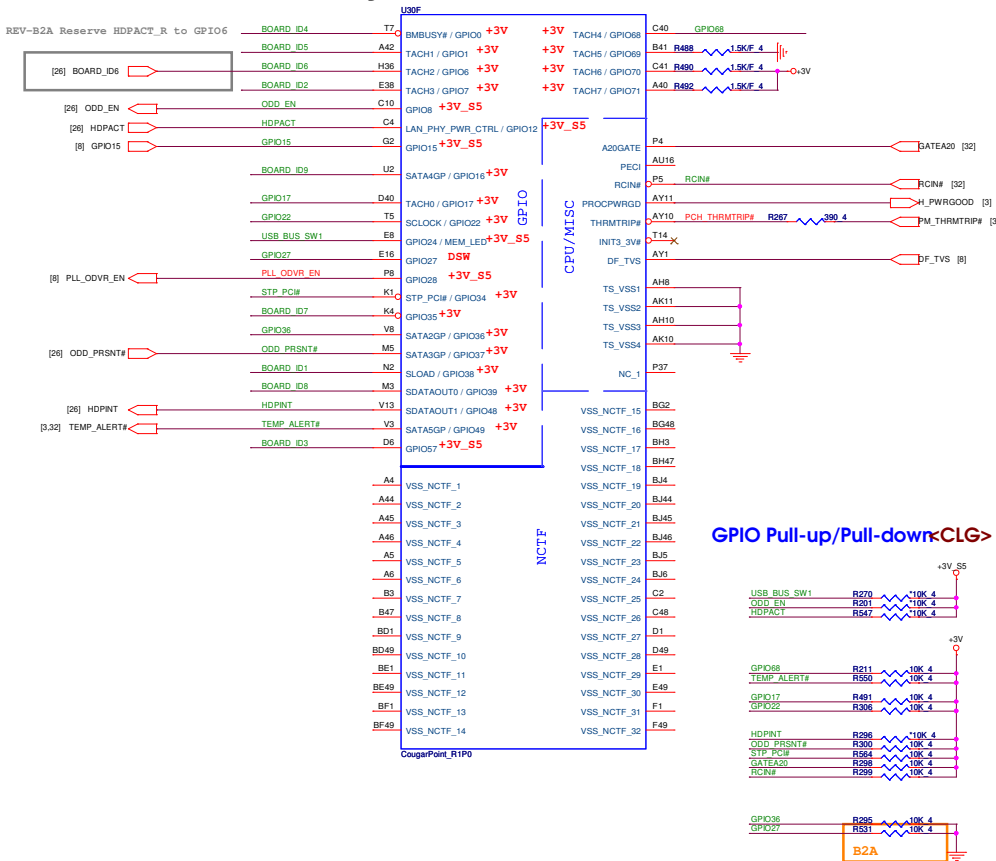
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWR0K	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	3V0 R581 1K.4 PCBEEP
GNT3# / GPIO55	Top-Block Swap Override	PWR0K	0 = Default (weak pull-up 20K) 1 = Setting to No-Reboot mode	R483 1K.4 PCI_GNT3# [9]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	3V RTC R513 330K.4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWR0K	0 = Default (weak pull-up 20K) 1 = Setting to No-Reboot mode	R479 1K.4 GNT1# [9]
GPIO19	Boot BIOS Selection 0 [bit-0]	PWR0K	0 = Default (weak pull-up 20K) 1 = Setting to No-Reboot mode	R560 1K.4 GPIO19
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	3V0 R498 1K.4 ACZ_SDOOUT ACZ_SDOOUT [25]
DF_TVS	DMI/FDI Termination voltage	PWR0K	0 = Set to Vcc 1 = Set to Vcc (weak pull-down 20K)	R543 238.4 DF_TVS [10]
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	3VPCU R571 1K.4 PLL_OOVR_EN [10]
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	3V_R50 R179 1K.4 ACZ_SYNC
GPIO15	TLS Confidentiality	RSMRST	0 = Default. TLS no Confidentiality 1 = TLS Confidentiality	3V_R50 R545 1K.4 GPIO15 [10]
DSWVRMEN	Deep S4/S5 Well On-Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable	3V_RTC R518 330K.4 R517 330K.4
INIT3_3V#	Reserved	PWR0K	1 = Default (weak pull-up 20K)	Should not pull low. leave as No Connect
GNT2# / GPIO53	ESI Strap (Server Only)	PWR0K	1 = Default. Should not be pulled low for desktop and mobile	Should not pull low for desktop and mobile
L_DDC_DATA	LVDS Detected	PWR0K	0 = Default. Not Detected 1 = Detected	1= PU to 3V
SDVO_CTRLDATA	Port B Detected	PWR0K	0 = Default. Not Detected 1 = Detected	1= PU to 3V
DDPC_CTRLDATA	Port C Detected	PWR0K	0 = Default. Not Detected 1 = Detected	0=NC
DDPD_CTRLDATA	Port D Detected	PWR0K	0 = Default. Not Detected 1 = Detected	0=NC
SATA3GP / GPIO37	Reserved	PWR0K	0 = Default	Should not be pulled high when strap is sampled
SATA2GP / GPIO36	Reserved	PWR0K	0 = Default	Should not be pulled high when strap is sampled

Cougar Point-M (PCI-E, SMBUS, CLK)



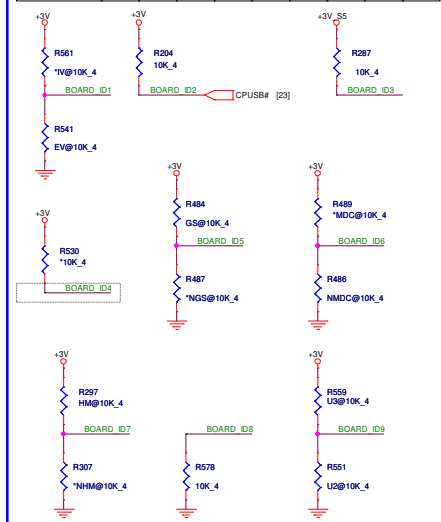
Cougar Point (GPIO, VSS_NCTF, RSVD)



BOARD ID SETTING

10

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID9
UMA SKU	H	L							
VGA SKU									
W/O 3G									
W/O 3G									
W/O LED KB									
W/O LED KB									
14"									
15"									
W G-SNR									
W/O G-SNR									
W/ MDC									
W/O MDC									
W/ HDMI									
W/O HDMI									
NC									
13"									
W/ USB3.0									
W/O USB3.0									



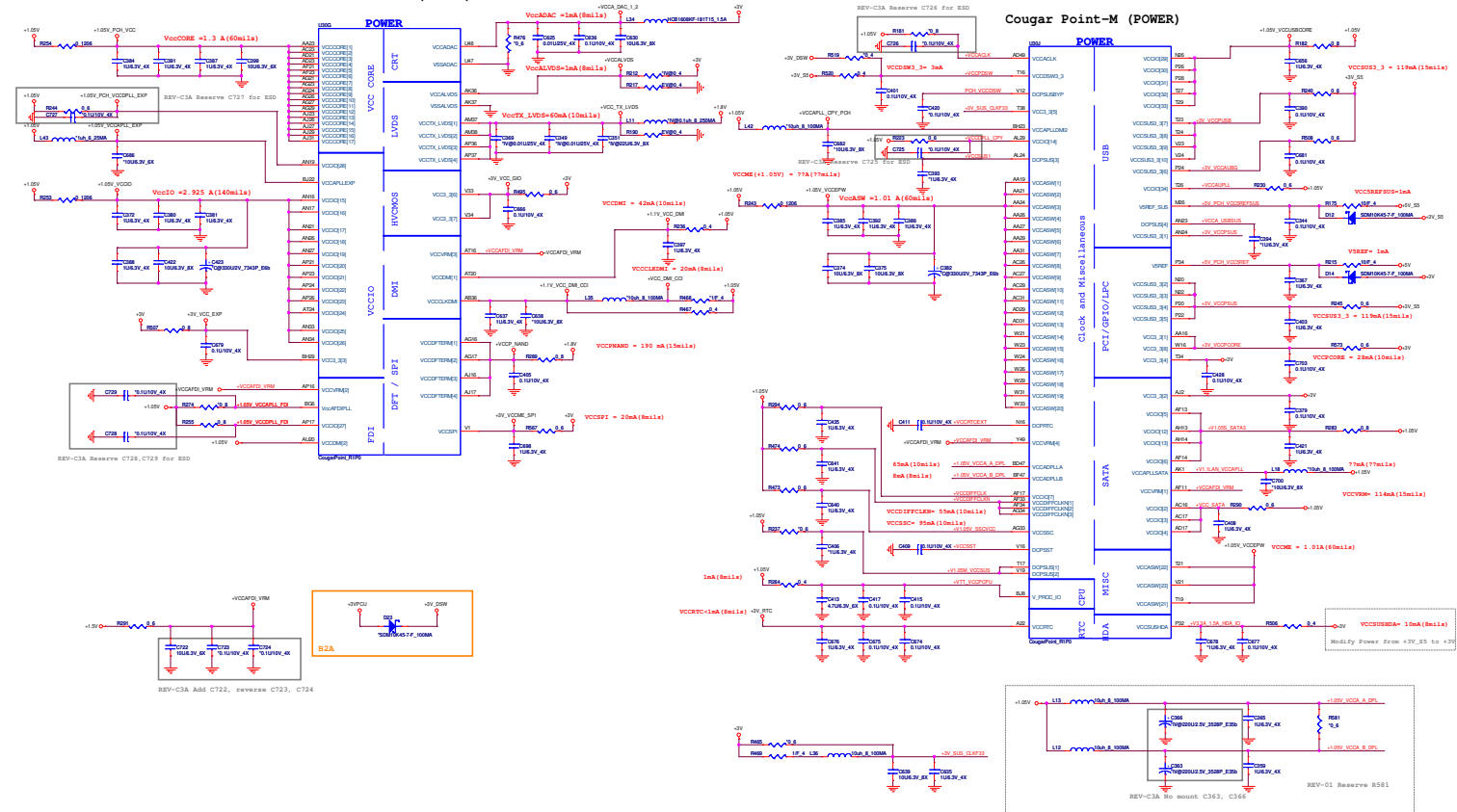
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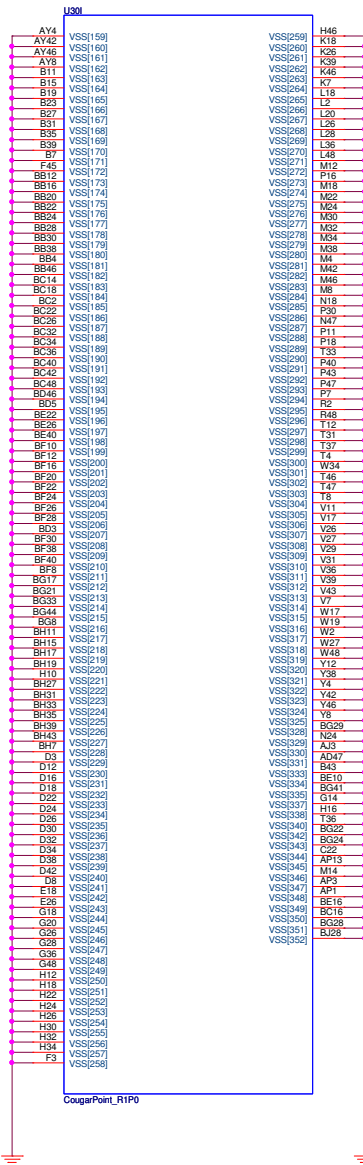
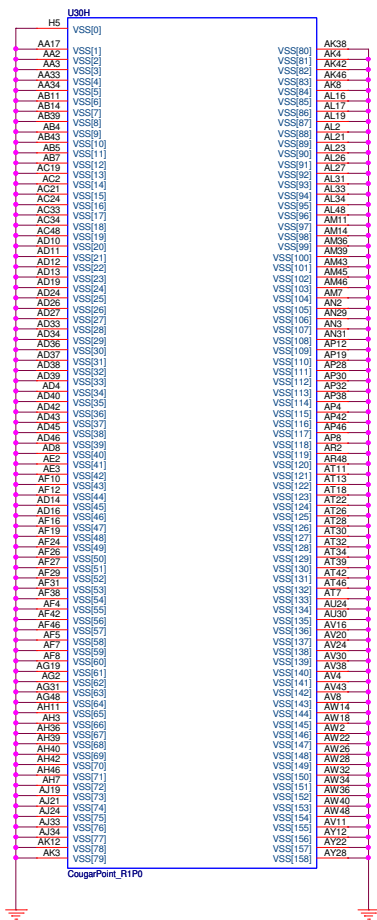
Cougar Point 4/6

Date: Tuesday, December 21, 2010

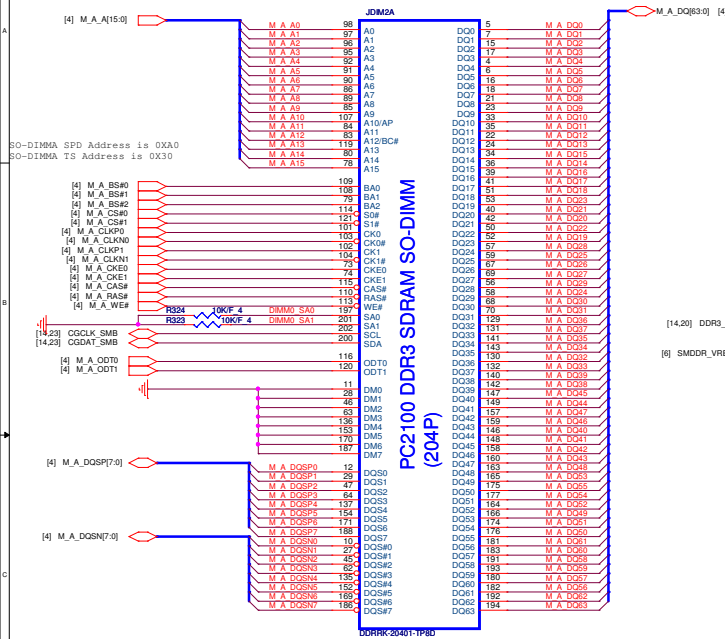
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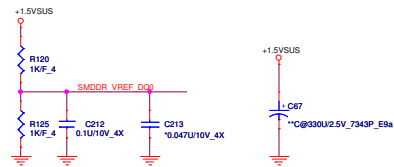
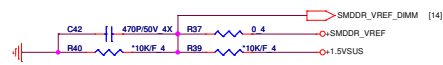
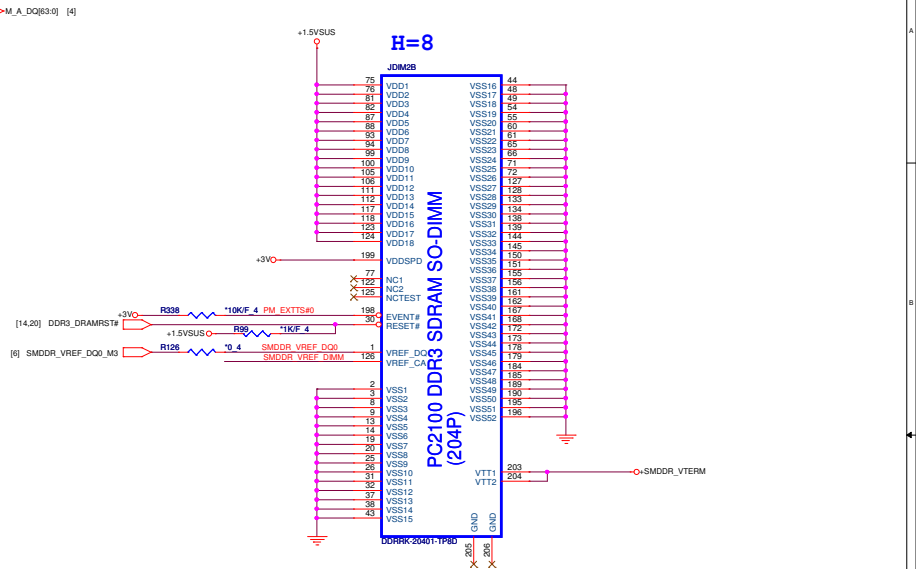
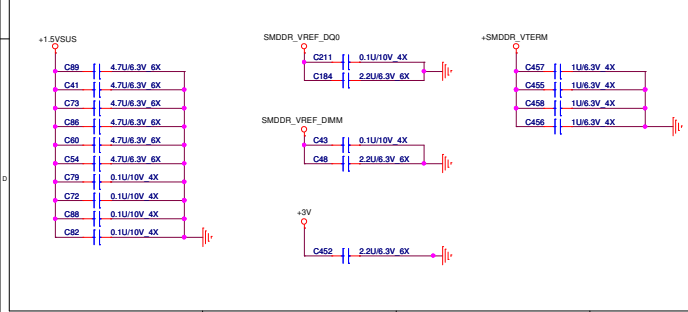
IBEX PEAK-M (GND)



H=8



Place these Caps near So-Dimm0.



H=4

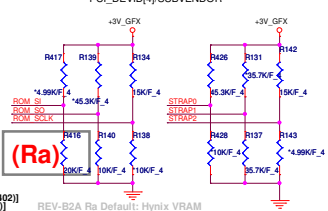




N12M-GE -> 0xA7A

1010 -> PU15K

Logical Strap Bit Mapping			
	PU-VDD	PD	
5K	1000	0000	
10K	1001	0001	
15K	1010	0010	
20K	1011	0011	
25K	1100	0100	
30K	1101	0101	
35K	1110	0110	
45K	1111	0111	



4.99K/F 4: CS34002F828 (RES CHIP 4.99K 1/16W +/-1% (0402))
10K/F 4: CS31002F828 (RES CHIP 10K 1/16W +/-1% (0402))
15K/F 4: CS31502F828 (RES CHIP 15K 1/16W +/-1% (0402))
20K/F 4: CS32002F828 (RES CHIP 20K 1/16W +/-1% (0402))
25K/F 4: CS32502F828 (RES CHIP 25K 1/16W +/-1% (0402))
30K/F 4: CS33002F828 (RES CHIP 30K 1/16W +/-1% (0402))
35K/F 4: CS33502F828 (RES CHIP 35K 1/16W +/-1% (0402))
45K/F 4: CS34502F828 (RES CHIP 45K 1/16W +/-1% (0402))

REV-B2A Ra Default: Hynix VRAM
REV-C3A Ra Default: Samsung VRAM 1Gbit

20K/F 4: CS32002F829 (RES CHIP 20K 1/16W +/-1% (0402))

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	XCLK_417 [0]	FB_0_BAR_SIZE [0]	SMB_ALT_ADDR [0]	VGA_DEVICE [1]
ROM_SCLK	PCI_DEVIDE[4] [1]	SUB_VENDOR [0]	SLOT_CLK_CFG [1]	PEX_PLL_EN_TERM [0]
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	PCI_DEVID[3] [1]	PCI_DEVID[2] [0]	PCI_DEVID[1] [1]	PCI_DEVID[0] [0]
STRAP1	3GIO_PADCFG[3][0]	3GIO_PADCFG[2][1]	3GIO_PADCFG[1][1]	3GIO_PADCFG[0][0]
STRAP0	USER[3] [1]	USER[2] [1]	USER[1] [1]	USER[0] [1]

VRAM Configuration Table


RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000		Reserved		
0010	DDR3 64Mx16x4pcs, 128bit, 512MB, 800MHz	Hynix		PD 15K
0011	DDR3 64Mx16x4pcs, 128bit, 512MB, 800MHz	Samsung		PD 20K
0110	DDR3 128Mx16x4pcs, 128bit, 1GB, 800MHz	Hynix		PD 35K
0111	DDR3 128Mx16x4pcs, 128bit, 1GB, 800MHz	Samsung		PD 45K
XXXX				

(Ra)

REV-B2A

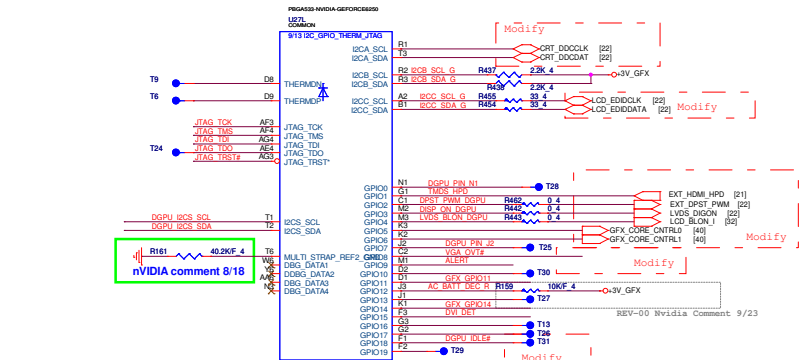
GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFF link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	NVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	Memory VREF SELECT
11	I/O	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	THERM_LOAD_STEP_DOWN
14	OUT	N/A	THERM_LOAD_STEP_UP

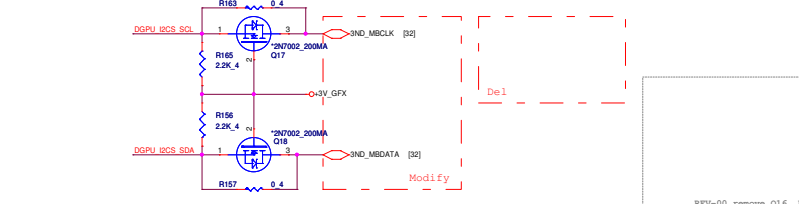
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Size	Document Number	
N12M-GE (GPIO/STRAPS)		
Date	Yvesley, December 21, 2019	Rev: 18 of 41

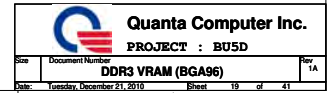


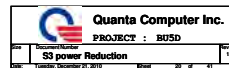
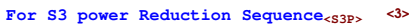
REV-C3A Modify test point footprint W25-T30 to TP3050

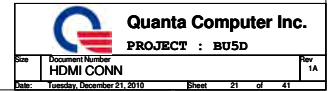


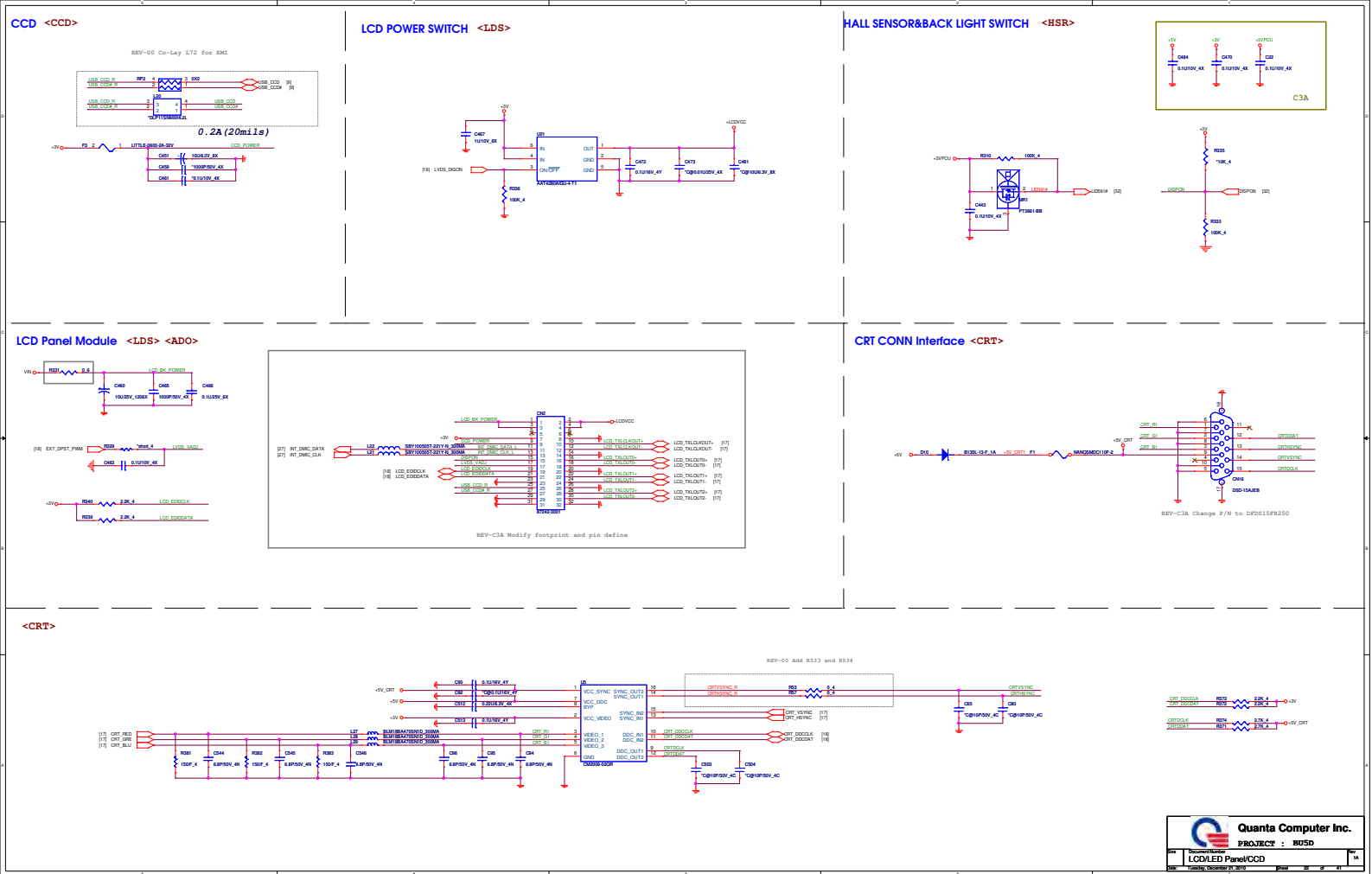
REV-00 remove Q16 , R71 and R70

[3,6,7,8,9,10,11,13,14,15,17,21,22,25,27,30,31,32,34,39]











USB 3.0 Controller <U3B>

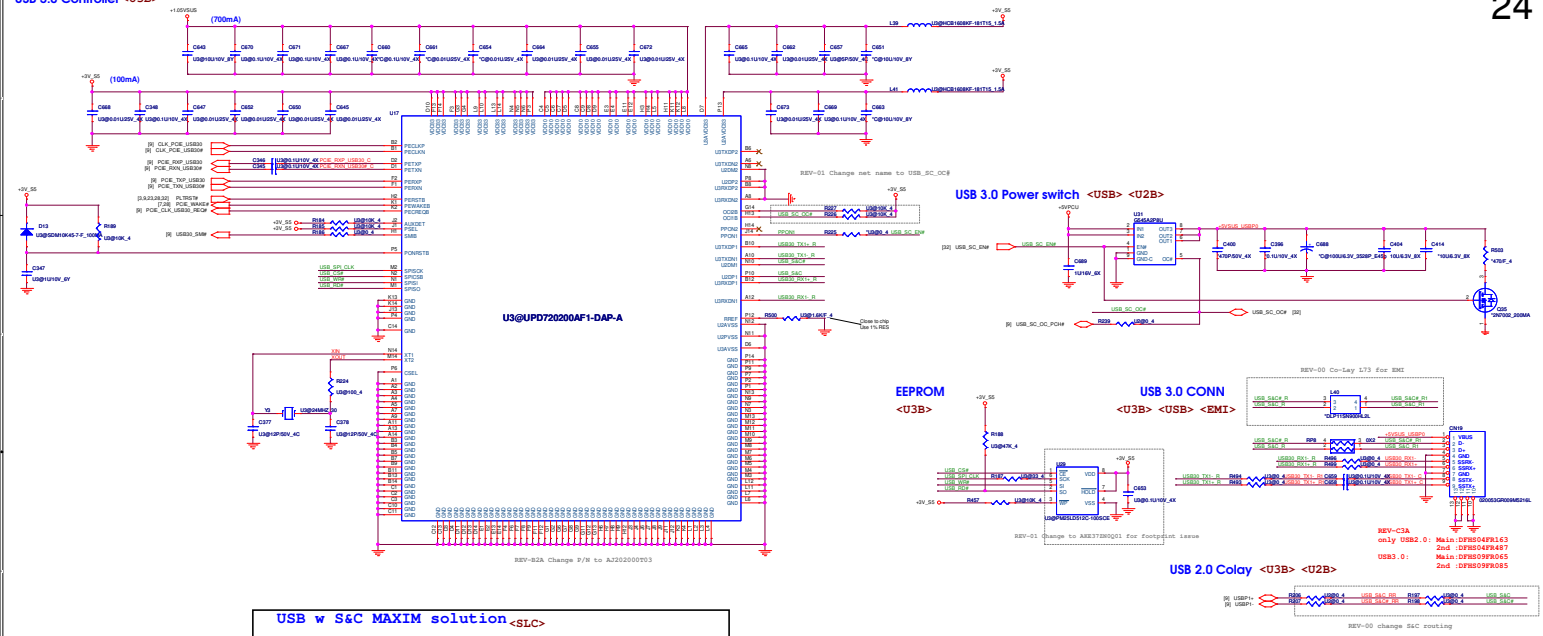
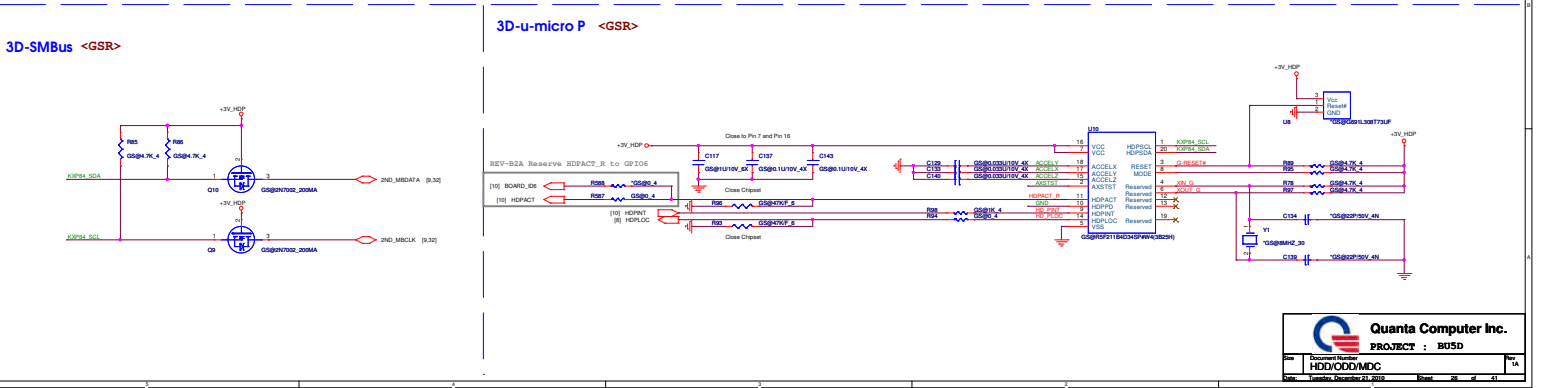
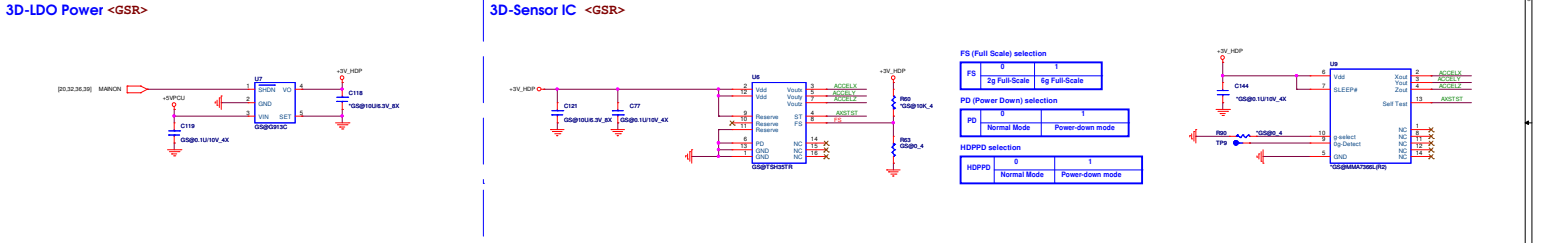
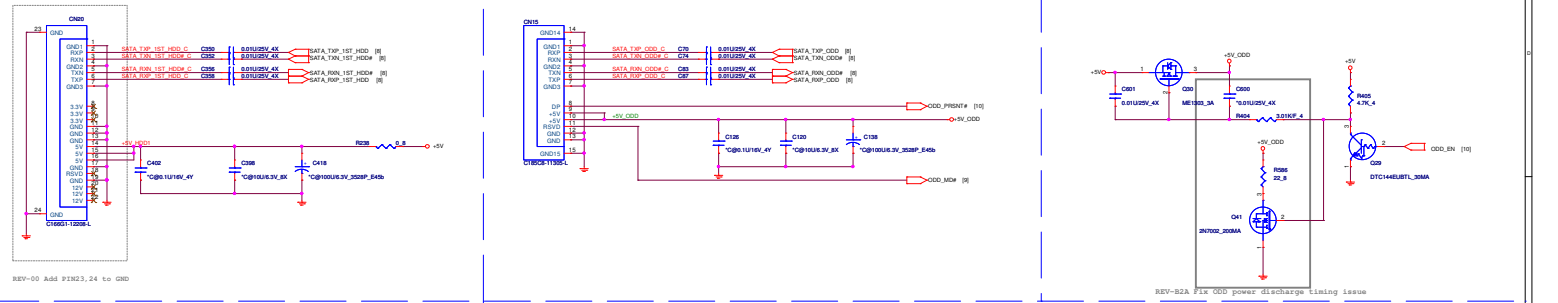
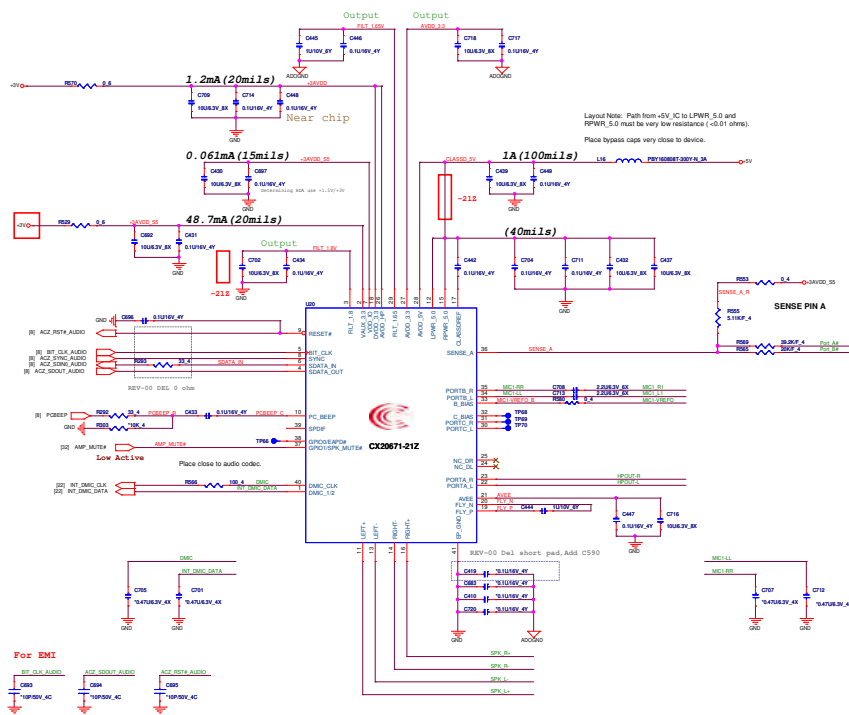


Figure 10: USB connector pin assignment. The diagram shows two views of a USB connector. The left view shows the internal wiring from the connector pins (CN6) to the board components (RP6, RP5, RP4, 48M_CARD, 3V, +5VDCU, REV-B2A Del R346 0 ohm). The right view shows the external wiring from the connector pins (L25, L24, L23) to the board components (USB_EXT1#, USB_EXT1, USB_EXT2#, USB_EXT2, USB_CARD#, USB_CARD, USB_CARD#, USB_CARD).

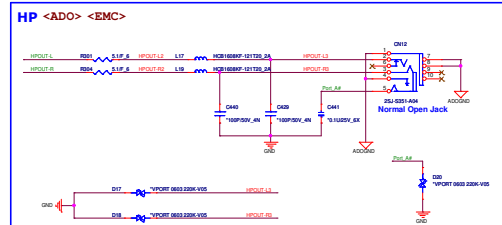
WWW.AliSaler.Com



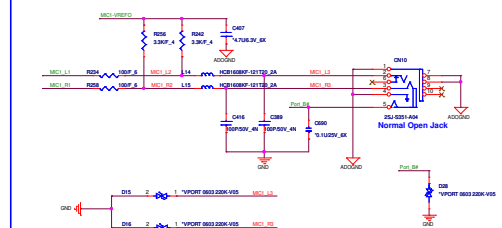
Codec (CX20671-21Z) <ADO>



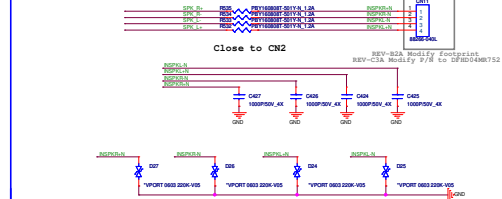
Need to change 20671-21Z footprint

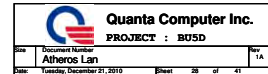
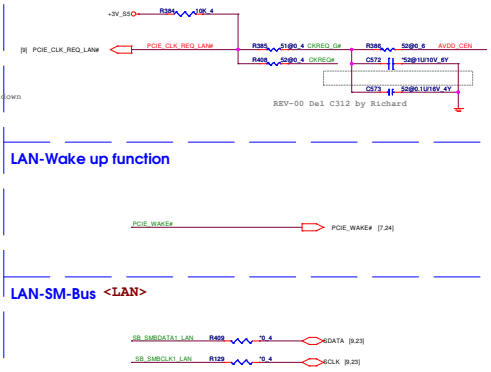


External MIC <ADO> <EMC>




Internal Speaker <ADO> <EMC>









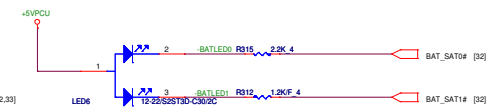
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PROJECT : BU5D

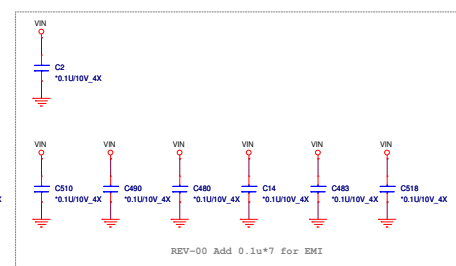
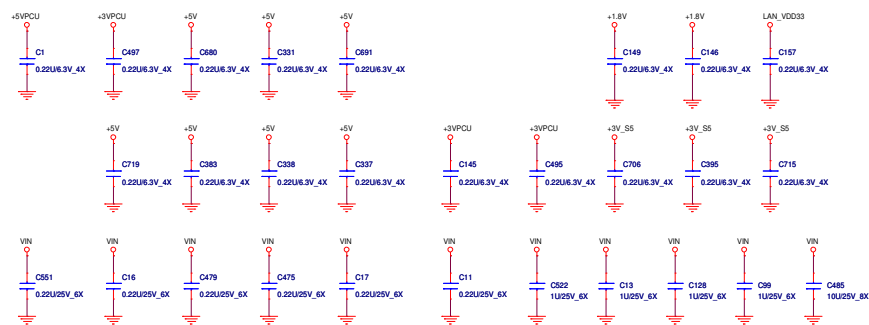
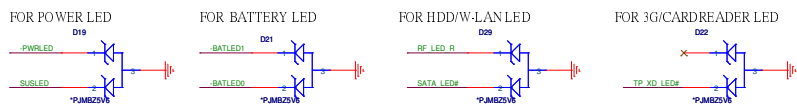
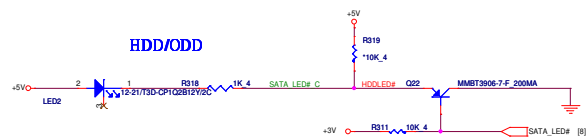
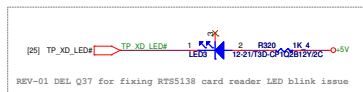
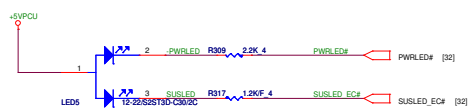
Card Reader (RTSS138)


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		1A
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D3A : LED luminance to light, 1K-ohm change 2.2K-ohm.

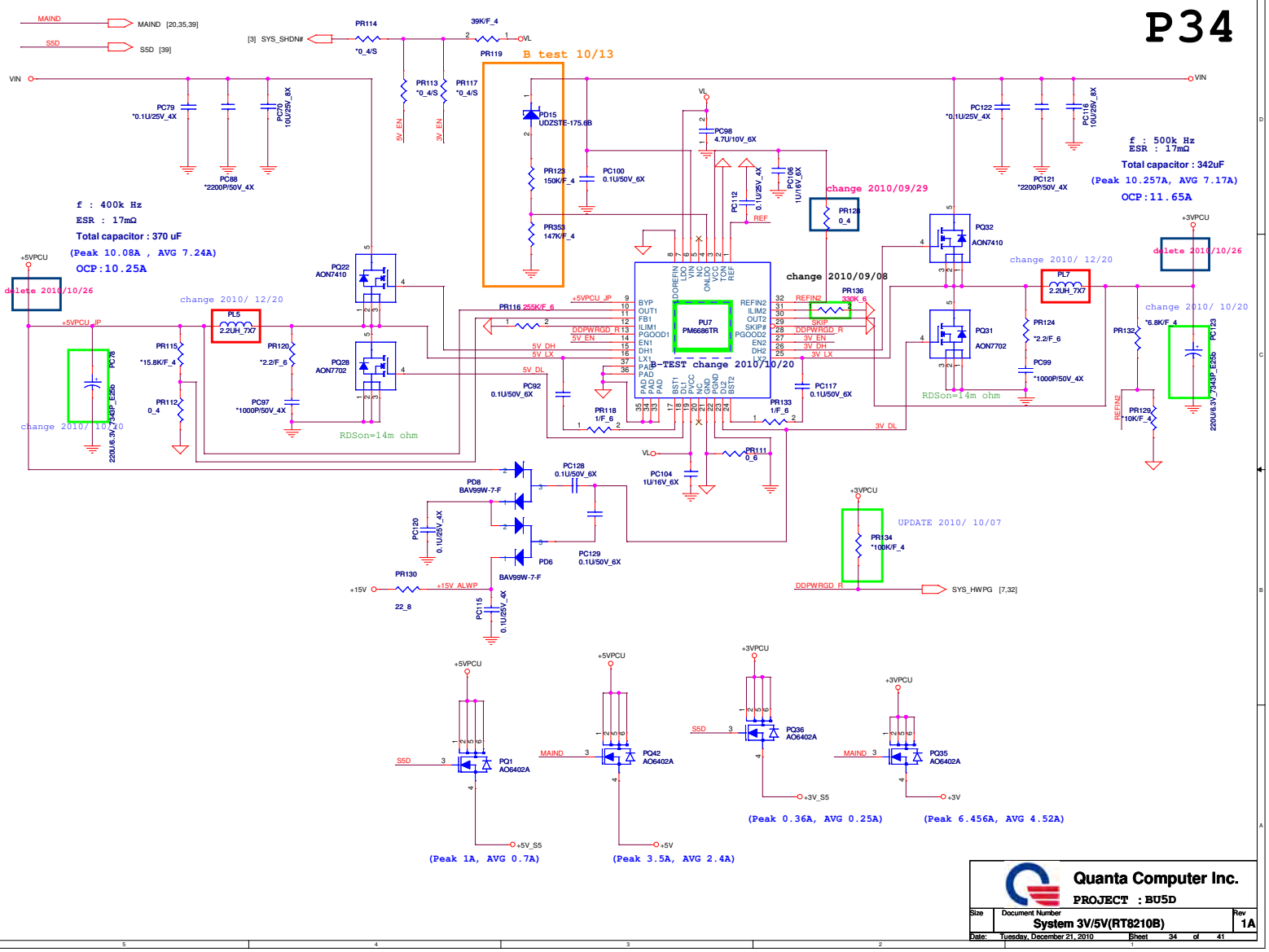


D3A : LED luminance to light,1K-ohm change 2.2K-ohm.

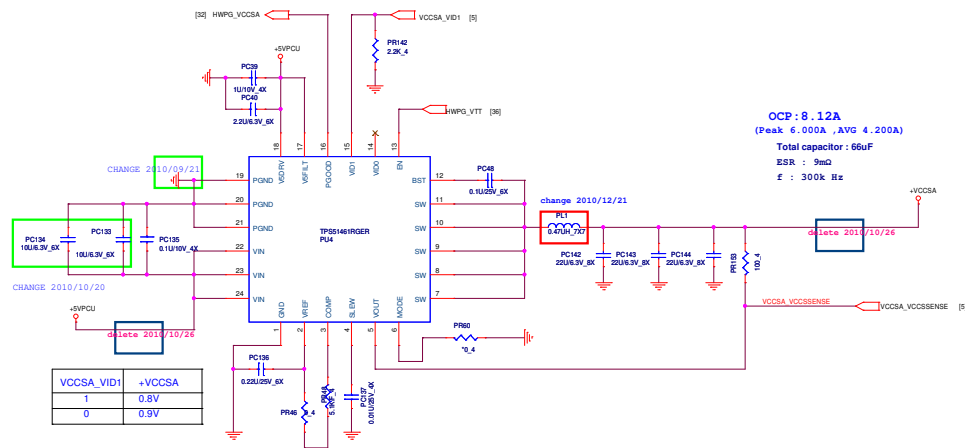


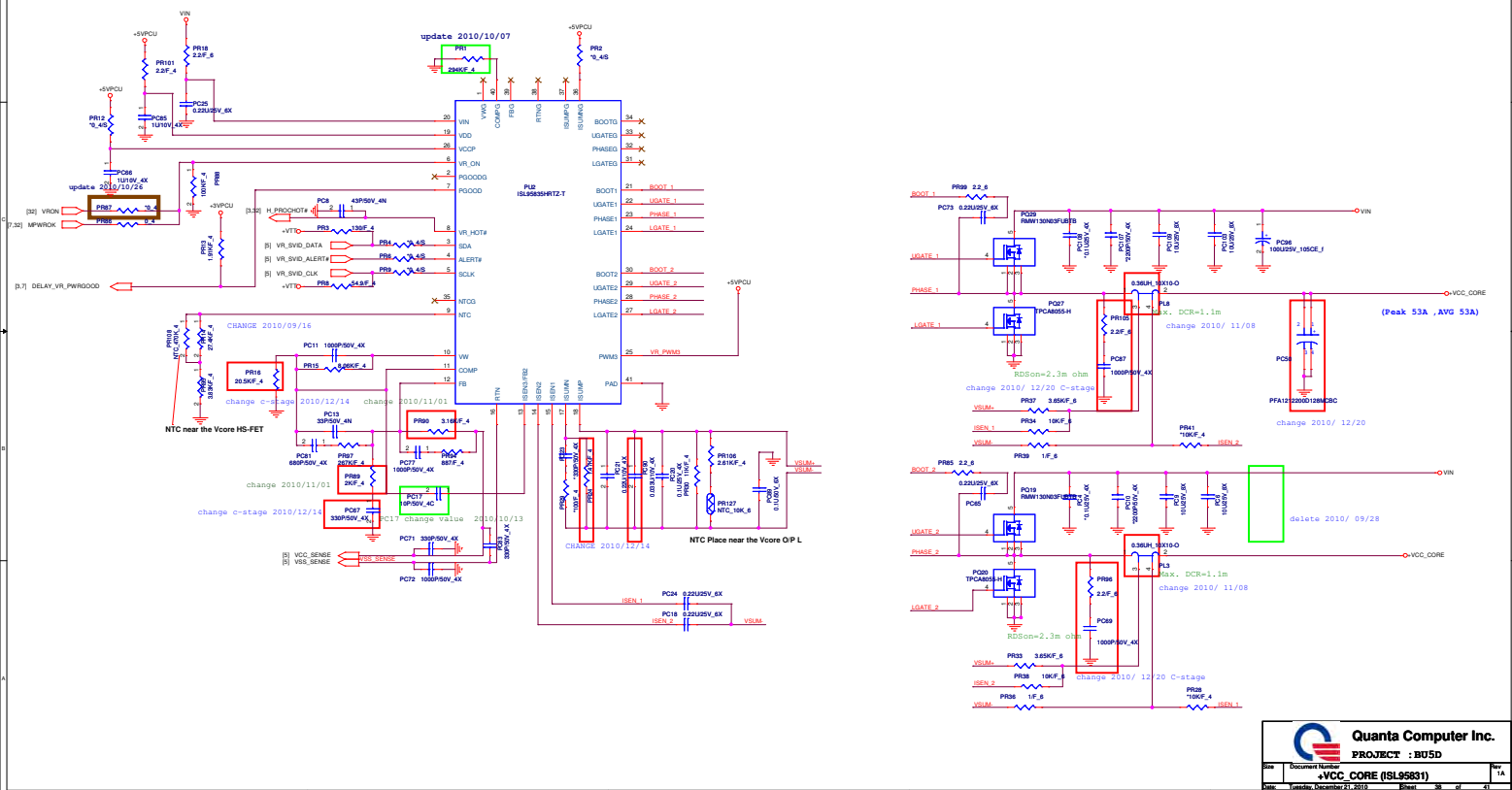
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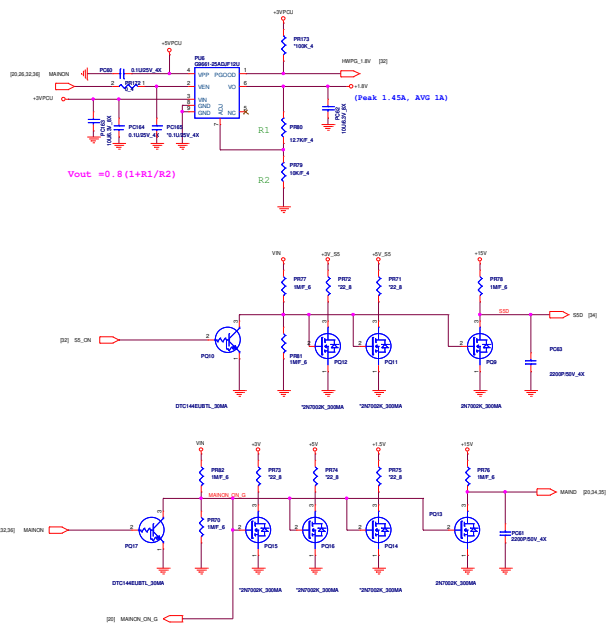


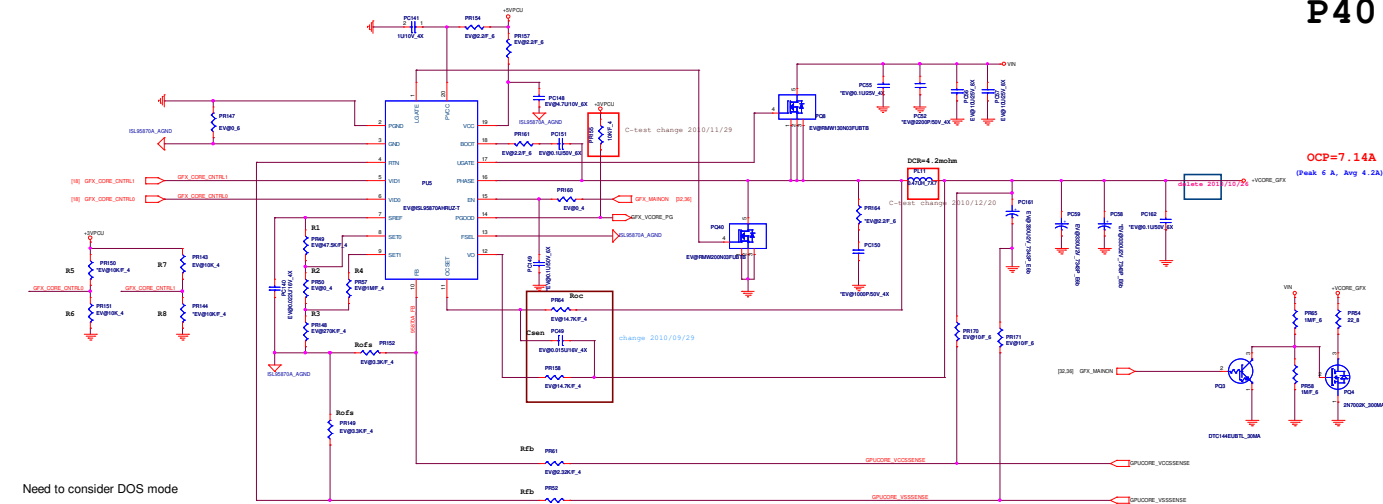












Default	N12P-LP	N12M-GE	N12P-GV
PR100	10K C3110023629	NC	10K C3110023629
PR101	NC	10K C3110023629	NC
PR102	10K C3110023629	NC	10K C3110023629
PR103	10K C3110023629	NC	10K C3110023629
PR104	10K C3110023629	NC	10K C3110023629

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	N12P-LP	N12M-GE	N12P-GV
LOW	LOW	0.905V	1.0V	0.98V
LOW	HIGH	0.90V Default	1.0V	0.98V
HIGH	LOW	0.9V	1.0V Default	0.98V
HIGH	HIGH	0.955V	0.98V	0.98V Default

B1	PR100	22.5K 4	C3110023610	27.5K 4	C3110023614	0.4	C3110023618
B2	PR101	0.4	C3110023610	0.4	C3110023614	0.4	C3110023618
B3	PR102	24.5K 4	C3110023610	27.5K 4	C3110023614	0.4	C3110023618
B4	PR103	24.5K 4	C3110023610	27.5K 4	C3110023614	0.4	C3110023618
B5	PR104	2.1K 4	C3110023610	2.3K 4	C3110023614	0.4	C3110023618
B6	PR105	2.2K 4	C3110023610	2.3K 4	C3110023614	0.4	C3110023618

